



Power Quotient International

— IC STORAGE SPECIALIST

## Preliminary

### **CompactFlash™** **32MB/64MB/96MB/128 MB/ 192MB/256MB/384MB/512MB**

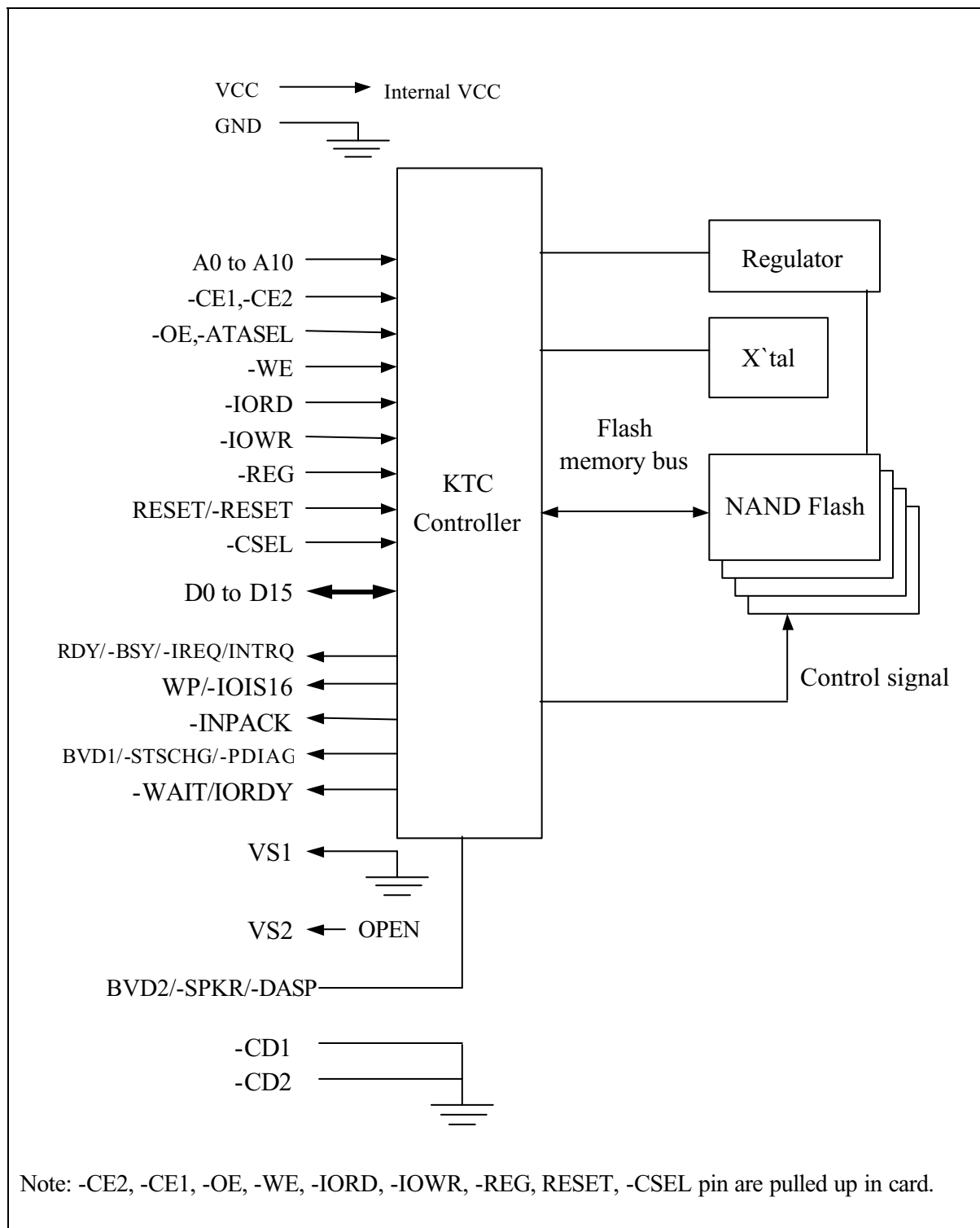
#### **Description**

The CompactFlash™ card complies with CompactFlash™ specification, and is suitable for the usage of data storage memory medium for PC or and other electric equipment and digital still camera. This card is equipped with NAND type flash memory. By using this card it is possible to operate good performance for the system which have CompactFlash™ slots.

#### **Features**

- CompactFlash™ specification standard
  - 50pin connector
  - Type I (3.3mm)
- 3.3V/5V single power supply operation
- Internal self-diagnostic program operates at Vcc power on
- 3 variations of mode access
  - Memory Card Mode
  - I/O Card Mode
  - True-IDE Mode
- High reliability based on internal ECC (Error Correcting Code) Function
- Data reliability is 1 error in 10<sup>14</sup> bits read
- Auto Sleep Mode

## Block Diagram



## Card Pin Assignment

Pin NO.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND		GND		GND	
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1		-CE1		-CE1	
8	A10		A10		A10	
9	-OE		-OE		-ATASEL	
10	A9		A9		A9	
11	A8		A8		A8	
12	A7		A7		A7	
13	VCC		VCC		VCC	
14	A6		A6		A6	
15	A5		A5		A5	
16	A4		A4		A4	
17	A3		A3		A3	
18	A2		A2		A2	
19	A1		A1		A1	
20	A0		A0		A0	
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O

Pin NO.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2		-CE2		-CE2	
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD		-IORD		-IORD	
35	-IOWR		-IOWR		-IOWR	
36	-WE		-WE		-WE	
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL		-CSEL		-CSEL	
40	-VS2	O	-VS2	O	-VS2	O
41	RESET		RESET		-RESET	
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	-INPACK	O
44	-REG		-REG		-REG	
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

# Host access specifications

## 1.Attribute access specifications

When CIS-ROM region or Configuration register region is accessed, read and write operations are executed under the condition of  $\text{-REG} = \text{"L"}$  as follows. That region can be accessed by Byte/Word/Odd -byte modes which are defined by PC card standard specifications.

### Attribute Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	High-Z	High-Z
Byte access(8-bit)	L	H	L	L	L	H	High-Z	even byte
	L	H	L	H	L	H	High-Z	invalid
Word access(16-bit)	L	L	L	×	L	H	invalid	even byte
Odd byte access(8-bit)	L	L	H	×	L	H	invalid	High-Z

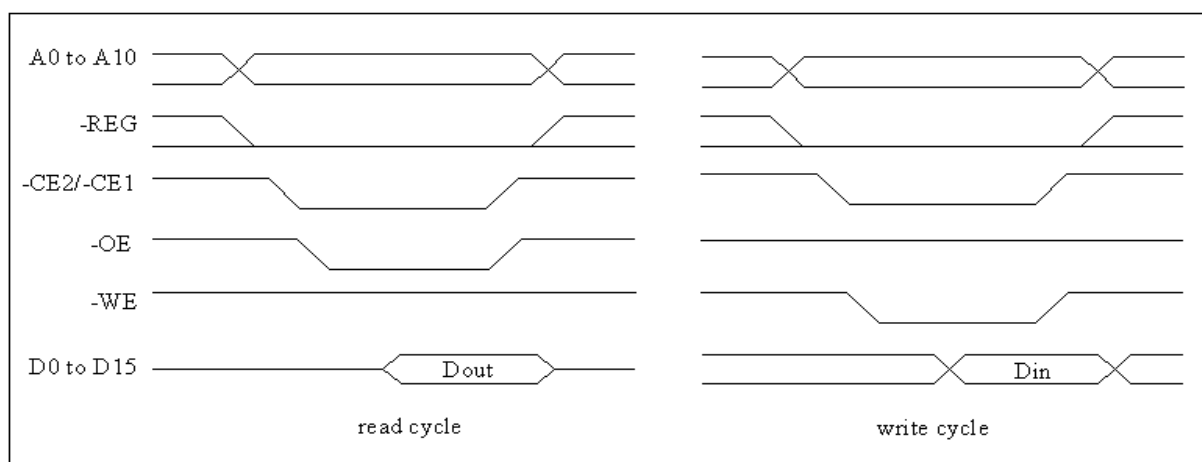
Note: × L or H

### Attribute Write Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	don't care	don't care
Byte access(8-bit)	L	H	L	L	H	L	don't care	even byte
	L	H	L	H	H	L	don't care	don't care
Word access(16-bit)	L	L	L	×	H	L	don't care	even byte
Odd byte access(8-bit)	L	L	H	×	H	L	don't care	don't care

Note: × L or H

### Attribute Access Timing Example



## 2.Task File register access specifications

There are two cases of Task File register mapping, one is mapped I/O address area, the other is mapped Memory address area. Each case of Task File register read and write operations are executed under the condition as follows. That area can be accessed by Byte/Word/Odd Byte mode which are defined by PC card standard specifications.

### (1)I/O address map

#### Task File Register Read Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access(8-bit)	L	H	L	L	L	H	H	H	High-Z	even byte
	L	H	L	H	L	H	H	H	High-Z	odd byte
Word access(16-bit)	L	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	×	L	H	H	H	odd byte	High-Z

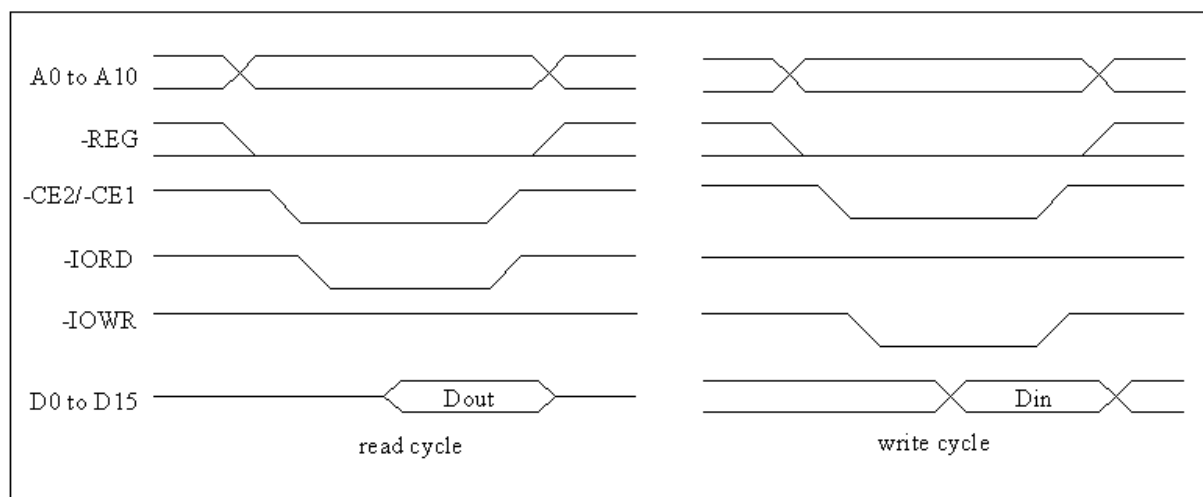
Note: × L or H

#### Task File Register Write Access Mode (1)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access(8-bit)	L	H	L	L	H	L	H	H	Don't care	even byte
	L	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	L	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	L	L	H	×	H	L	H	H	odd byte	don't care

Note: × L or H

#### Task File Register Access Timing Example (1)



## (2)Memory address map

### Task File Register Read Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	High-Z	High-Z
Byte access(8-bit)	H	H	L	L	L	H	H	H	High-Z	even byte
	H	H	L	H	L	H	H	H	High-Z	odd byte
Word access(16-bit)	H	L	L	×	L	H	H	H	odd byte	even byte
Odd byte access(8-bit)	H	L	H	×	L	H	H	H	odd byte	High-Z

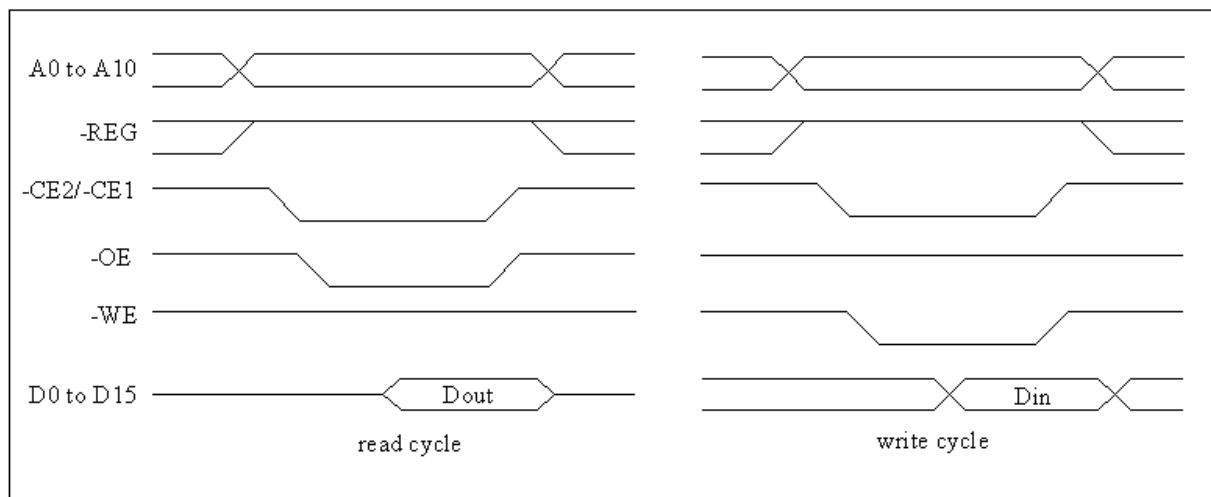
Note: × L or H

### Task File Register Write Access Mode (2)

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D8 to D15	D0 to D7
Standby mode	×	H	H	×	×	×	×	×	Don't care	Don't care
Byte access(8-bit)	H	H	L	L	H	L	H	H	Don't care	even byte
	H	H	L	H	H	L	H	H	Don't care	odd byte
Word access(16-bit)	H	L	L	×	H	L	H	H	odd byte	even byte
Odd byte access(8-bit)	H	L	H	×	H	L	H	H	odd byte	don't care

Note: × L or H

### Task File Register Access Timing Example (2)



### 3.True IDE Mode

The card can be configured in a True IDE Mode of operation. This card is configured in this mode only when the  $\overline{\text{OE}}$  input signal is asserted GND by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration is disabled and only I/O operations to the Task File and Data Register and allowed. In this mode no Memory or Attribute Registers are accessible to the host. The card permit 8 bit accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

#### True IDE Mode Read I/O Function

Mode	$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	A0 to A2	$\overline{\text{IORD}}$	$\overline{\text{IOWR}}$	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	High-Z	High-Z
Standby mode	H	H	×	×	×	High-Z	High-Z
Data register access	H	L	0	L	H	Odd byte	even byte
All status access	L	H	6H	L	H	High-Z	Status out
Other task file access	H	L	1-7H	L	H	High-Z	data

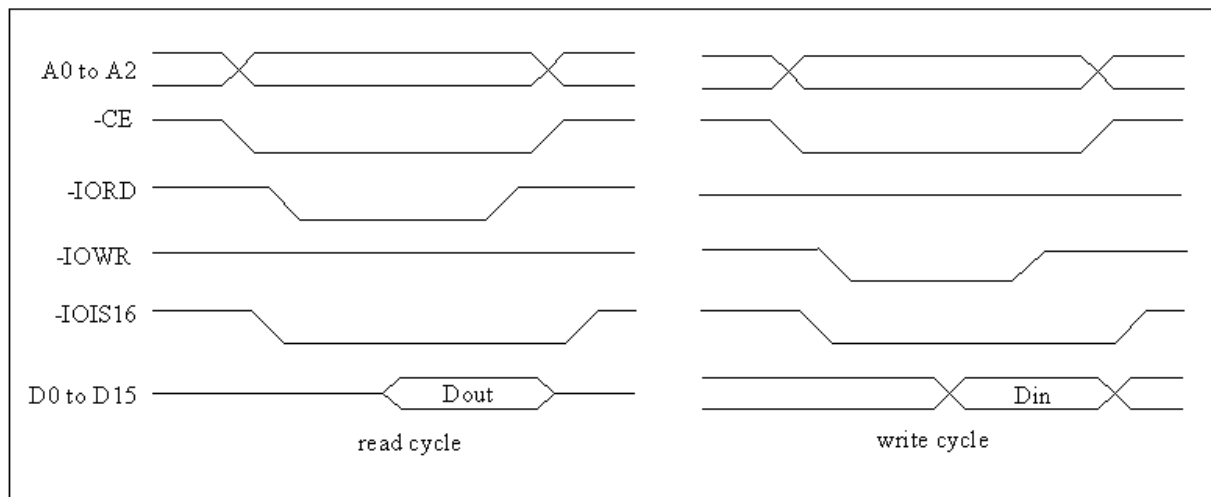
Note: × L or H

#### True IDE Mode Write I/O Function

Mode	$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	A0 to A2	$\overline{\text{IORD}}$	$\overline{\text{IOWR}}$	D8 to D15	D0 to D7
Invalid mode	L	L	×	×	×	don't care	don't care
Standby mode	H	H	×	×	×	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control
Other task file access	H	L	1-7H	H	L	don't care	data

Note: × L or H

#### True IDE Mode I/O Access Timing Example



## Configuration register specifications

This card supports four Configuration registers for the purpose of the configuration and observation of this card.

### 1. Configuration Option register (Address 200H)

This register is used for the configuration of the card configuration status and for the issuing soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevIREQ	INDEX					

Note: initial value: 00H

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to “1”, places the card in the reset state (Card Hard Reset). This operation is equal to Hard Reset, except this bit is not cleared. Then this bit set to “0”, places the card in the reset state of Hard Reset (This bit is set to “0” by Hard Reset). Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.
LevIREQ (HOST->)	R/W	This bit sets to “0” when pulse mode interrupt is selected, and “1” when level mode interrupt is selected.
INDEX (HOST->)	R/W	This bits is used for select operation mode of the card as follows. When Power on, Card Hard Reset and Soft Reset, this data is “000000” for the purpose of Memory card interface recognition.

### INDEX bit assignment

INDEX bit						Card mode	Task File register address	Mapping mode
5	4	3	2	1	0			
0	0	0	0	0	0	Memory card	0H to FH, 400H to 7FFH	memory mapped
0	0	0	0	0	1	I/O card	××0H to ××FH	Contiguous I/O mapped
0	0	0	0	1	0	I/O card	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	I/O card	170H to 177H, 376H to 377H	Secondary I/O mapped

## 2.Configuration and Status register (Address 202H)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0

Note: initial value: 00H

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY-BSY bit on Pin Replacement register is set to "1". When CHGED bit is set to "1", -STSCHG pin is held "L" at the condition of SIGCHG bit set to "1" and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status-change signal (-STSCHG pin). When the card is configured I/O card interface and this bit is set to "1", -STSCHG pin is controlled by CHGED bit. If this bit is set to "0", -STSCHG pin is kept "H".
IOIS8 (HOST->)	R/W	The host sets this field to "1" when it can provide I/O cycles only with on 8bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to "1", the card enters sleep state (Power Down mode). When this bit is reset to "0", the card transfers to idle state (active mode). RRDY/-BSY bit on Pin Replacement Register becomes BUSY when this bit is changed. RRDY/-BSY will not become Ready until the power state requested has been entered. This card automatically powers down when it is idle, and powers back up when it receives a command.
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. This bit state is available whether I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero.

### 3.Pin Replacement register (Address 204H)

This register is used for providing the signal state of –IREQ signal when the card configured I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	0	1	1	RRDY/-BSY	0

Note: initial value: 00H

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to “1” when the RRDY/-BSY bit changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	When read, this bit indicates +READY pin states. When written, this bit is used for CRDY/-Bsy bit masking.

### 4.Socket and Copy register (Address 206H)

This register is used for identification of the card from the other card. Host can read and write this register. This register should be set by host before this card’s Configuration Option register set.

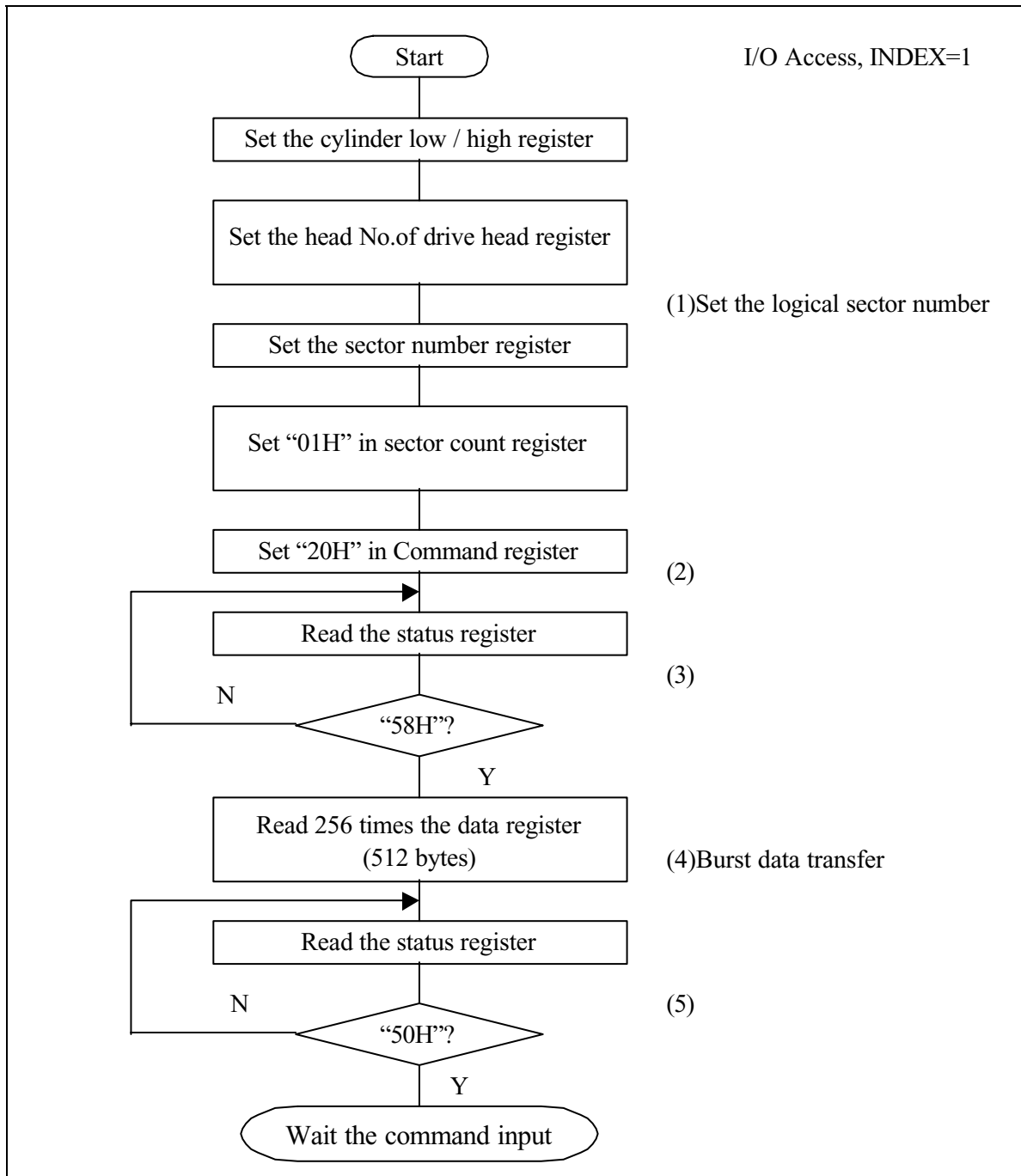
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	0	0	0	0

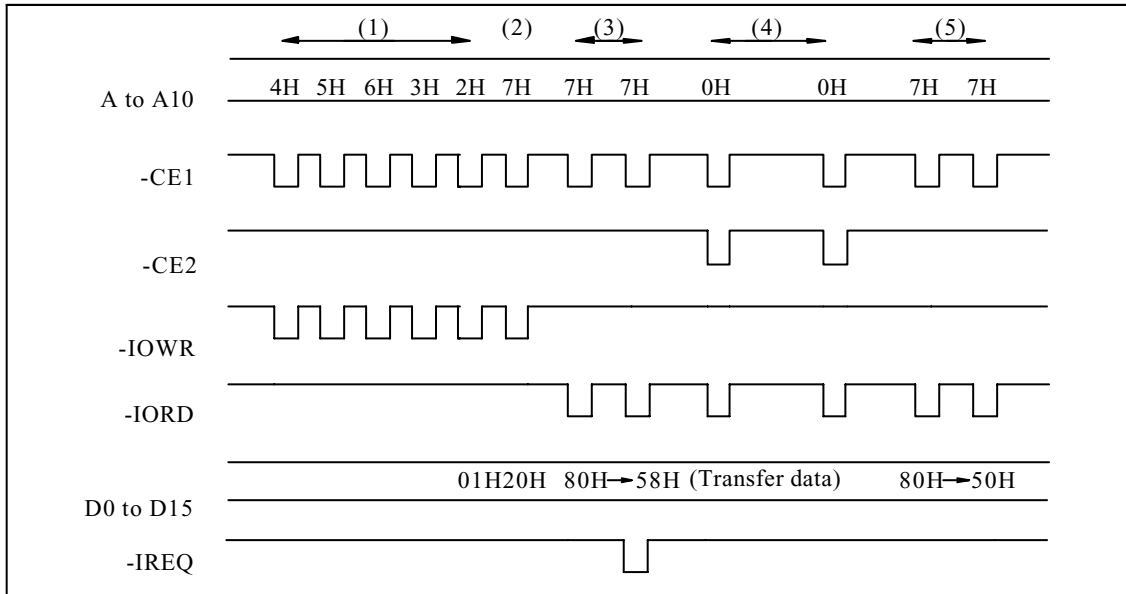
Note: initial value: 00H

Name	R/W	Function
DRV# (HOST->)	R/W	This fields are used for the configuration of the plural cards. When host configures the plural cards, written the card’s copy number in this field. In this way, host can perform the card’s master/slave organization.

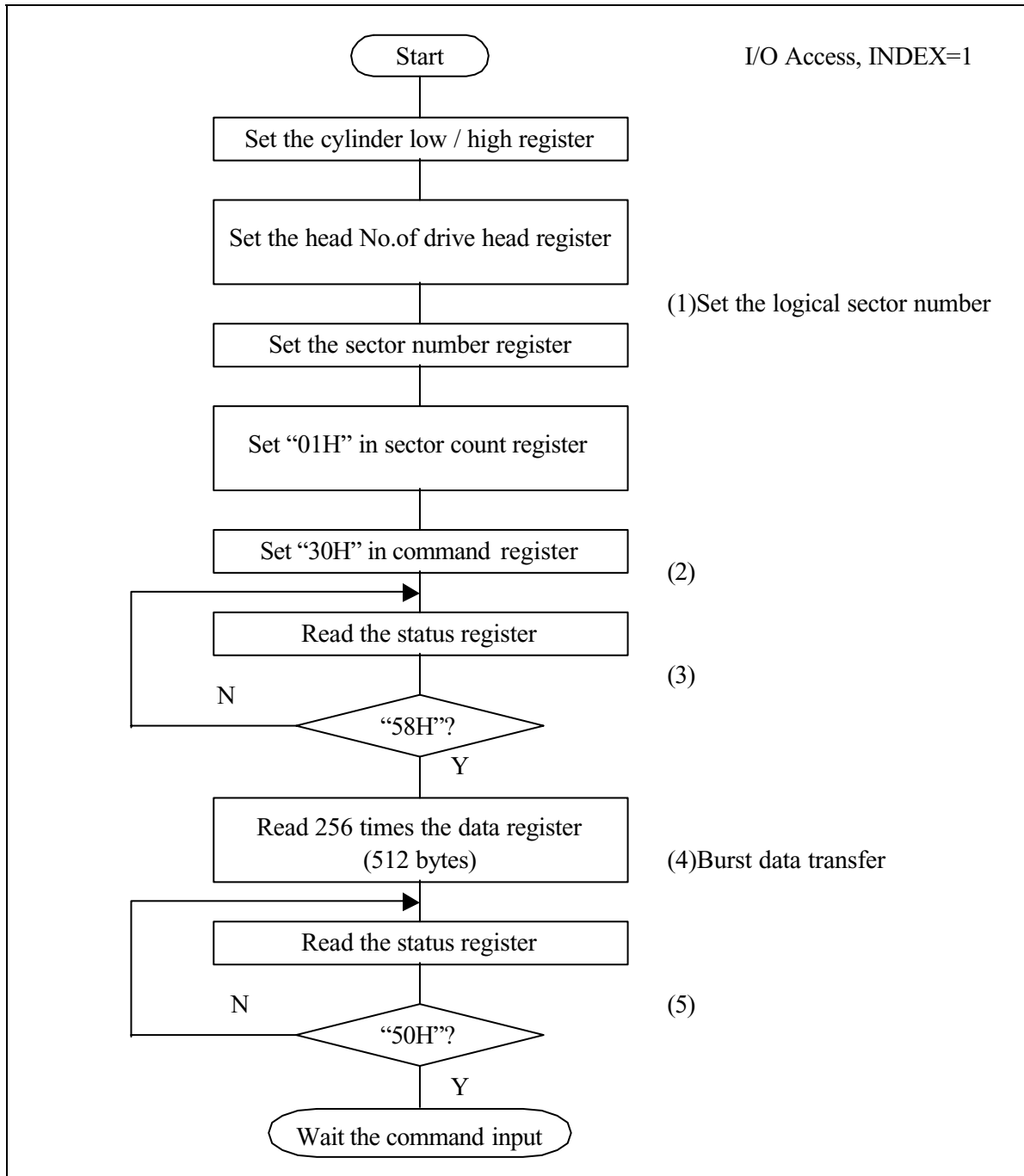
# Sector Transfer Protocol

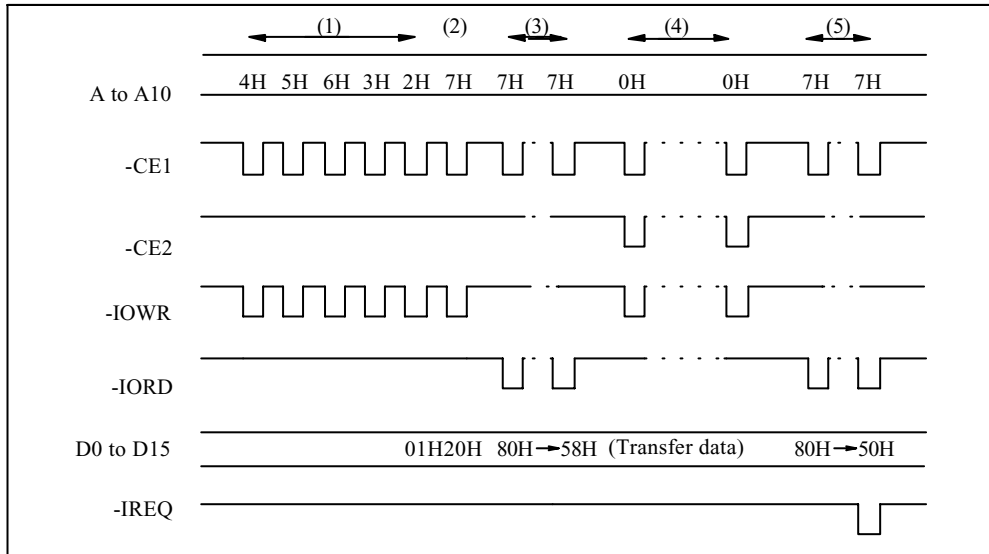
1. Sector read: 1 sector read procedure after the card configured I/O interface is shown as follows.





2. Sector write: 1 sector write procedure after the card configured I/O interface is shown as follows.





# Physical Outline

Unit: mm

